# *CRESCENT HEART SOFTWARE*

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TF-GBE

GIGABIT ETHERNET COMPLIANCE TEST FIXTURE

FOR USE WITH

TEKTRONIX TDSET2

ETHERNET COMPLIANCE TEST SOFTWARE

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**REFERENCE GUIDE**

**Version 1.2.1**

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Please communicate suggestions for product and documentation improvements to the technical support e-mail address above.

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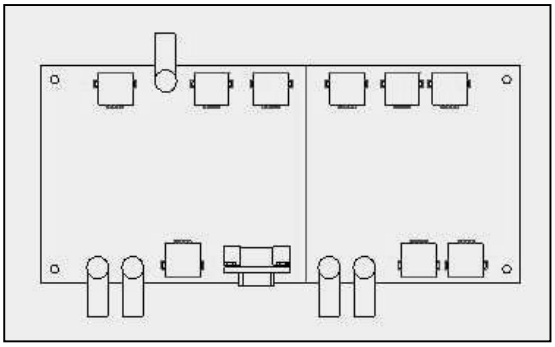
# 1. General Information

## 1.1 TF-GBE Product Features

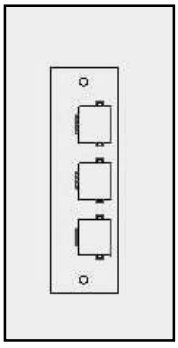
The TF-GBE offers following capabilities:

- Support for 1000/100/10BaseT technologies enables comprehensive testing
- Support for wide spectrum of tests saves time
- On-board test points for accurate removal of disturbing signals ensures reliable results
- Special Return Loss Calibration Board shrinks time taken for testing
- Test Channel for 1000BaseT Jitter tests ensures tests as per standard
- Cross-connect circuits simplify connection to traffic generators and link partners
- Twisted-Pair-Model and Loads (as per IEEE802.3) enables complete transmitter testing of 10BaseT Physical Layer

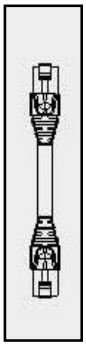
## 1.2 Supplied Components



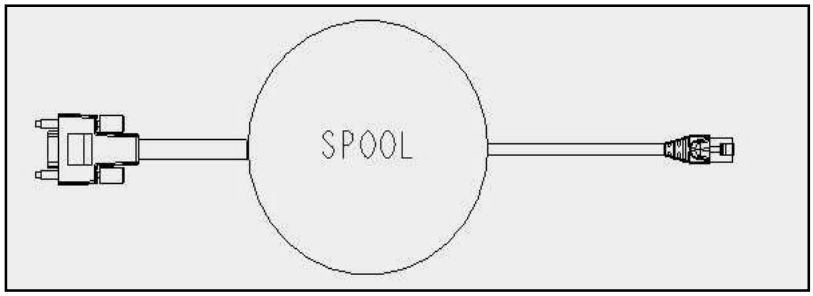
**Main PCB**



**Return Loss Calibration PCB**



**Short RJ45 Interconnect Cable**




**Jitter Test Channel Cable (available as TF-GBE-JTC or standard on TF-GBE-ATP)**

## 1.3 TF-GBE Specifications

### 1.3.1 1000Base-T Tests Supported

- Templates - all pairs
- Peak Voltage - all pairs
- Level Accuracies - all pairs
- Jitter – Test Channel; D-conn to RJ45 interface
- Distortion – all pairs
- Common Mode Output Voltage – all pairs
- Return Loss – all pairs; Calibration Circuits included

### 1.3.2 100BaseTX Tests Supported

- Template
- Amplitude Domain – Output Voltage, Amplitude Symmetry, Overshoot
- Time Domain – Rise time, Fall Time, Rise/Fall Symmetry
- Jitter Domain – Total Jitter, Duty-Cycle-Distortion
- Common Mode Output Voltage
- Return Loss – Tx, Rx; Calibration Circuits included

### 1.3.3 10BaseT Tests Supported

- Link Pulse Template – w/TPM and w/0 TPM, Loads 1, 2 and 100Ω
- TP_IDL Template - w/TPM and w/0 TPM, Loads 1, 2 and 100Ω
- MAU Template – with TPM (Twisted Pair Model)
- Output Voltage Amplitude
- Harmonic of Ones or Zeros
- Jitter
- Common Mode Output Voltage
- Return Loss – Tx, Rx; Calibration Circuits included

## 1.4 Oscilloscope Requirements

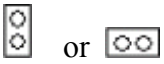
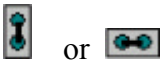
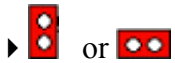
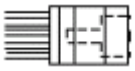
The TF-GBE Test Fixture is designed for use with TDSET2 Ethernet Compliance Test Software running on following oscilloscopes from Tektronix:

- TDS6000 series: TDS6404, TDS6604
- TDS7000 series: TDS7054, TDS7104, TDS7154, TDS7254, TDS7404
- CSA7000 series: CSA7154, CSA7404

For more details on ordering and configurations, contact Tektronix sales or visit **www.tektronix.com**.

## 1.5 Document Conventions

**Table 1.1: Test Fixture Notation and Description**

| Notation | Description |
|---|---|
|  | Open Jumpers |
|  | Short Jumpers |
|  | Probe Points (align ▸ with '+' lead of the differential probe) |
|  | RJ45 Ethernet Cable |
| | RJ45 Ethernet Port |

# 2 About TDSET2 Ethernet Compliance Test Software

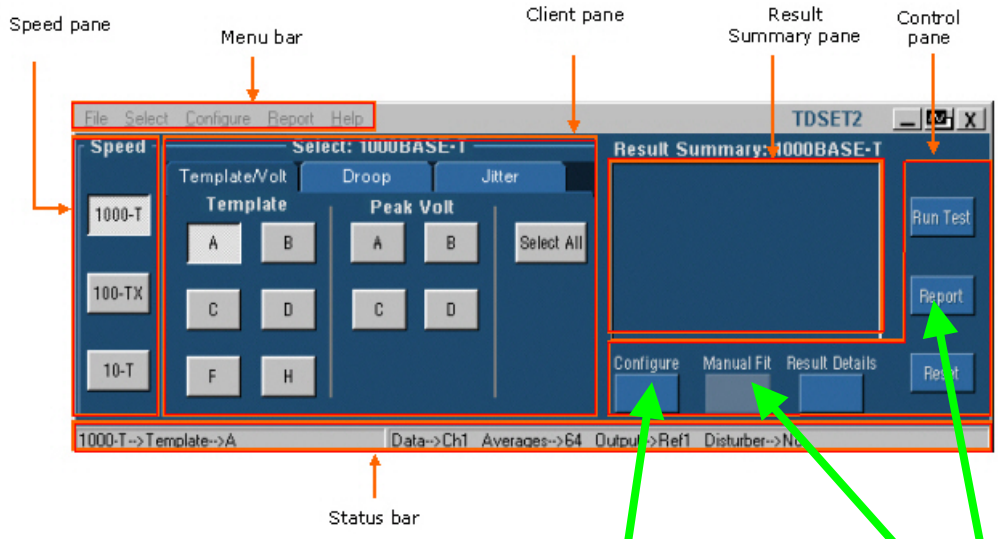
## 2.1 General Capabilities

The TDSET2 Ethernet Compliance Test Software from Tektronix, coupled with TDS/CSA7000 and TDS6000 Series oscilloscopes, enhances efficiency with faster validation cycles and much higher reliability. Key features of TDSET2 software are:

- Wide range of tests for 10/100/1000BaseT enables complete compliance to standards
- Ingenious "Select All" feature ensures faster testing with much reliability
- Automatic Pass/Fail notification delivers quick results
- Auto-fit process minimizes time for testing
- Locate and Flash Hits pinpoint mask hits for efficient debug
- Automated Jitter measurements eliminate human intervention for faster and reliable measurements
- Sophisticated "One-button" report generator saves precious time

## 2.2 Introduction to TDSET2 version 1.30

The TDSET2 is laid out in distinct panes as described below:




☞ **Key things to remember:**

1. "Select" and "Configure" functions are a single toggle button.
2. If auto-fit has not fitted the signal perfectly, you may use "Manual Fit". Manual fit is enabled only for template tests.
3. The one-button report generator would auto-increment file name/number.
   For repeatable and reliable results, refer section 3.

## 2.3 Setups for reliable results

Remember that the margins specified in Ethernet standards are very tight. While testing, it is important to pay special attention to many aspects of the test setup. The key contributors to unreliable measurements are:

1. Non-linearities in the acquisition path: The test margins are very narrow and any non-linearity can affect the measurement adversely. The following steps would ensure reliable measurements:
   - Signal Path Compensation (SPC) on the oscilloscope. Refer oscilloscope user manual for details on how to perform SPC.
   - Probe calibration is highly recommended prior to performing the tests. Refer oscilloscope user manual for details.
   - JigMatch ensures that the disturber and fixture non-linearities are compensated while testing. Refer section 2.2.1 for procedures.
2. Noise: By far, noise is the biggest contributor for erroneous or doubtful results. The following precautions minimize noise:
   - Keep interconnects as small as possible. The TF-GBE-SIC ensures short interconnects.
   - Ensure that the probe stays away from power supply of the DUT.
   - Un-terminated interconnects in circuits can act as excellent transmitters. Either remove them or terminate such interconnects.
   - In the configure menu for each test, check for the numbers of averages:
     - For 1000BaseT Template/Amplitude/Droop tests, set averages to 64 or more
     - For 100BaseTX, set averages to 16 or more for all tests (except for template and Jitter tests, where it is not applicable)
     - For 10BaseT, set averages to 16 or more for Link Pulse Test

***NOTE.*** *For 100BaseTX template test and MAU-Template test for 10BaseT, define the number of samples to at least 50,000. You can do this by selecting the Configure button in Control pane and then selecting the Mask Configuration button.*

## 2.4 Test-to-Fixture Matrix

The following chart provides a cross-matrix of tests and test-circuits on the fixture.

**Table 2.1: Test-to-Fixture Matrix**

| | Compliance Test | TC1 | TC2 | TC3 | TC4 | TC5 | TC6 | TC7 | RLCF[1] | JTC[2] |
|---|---|---|---|---|---|---|---|---|---|---|
| 1000 | Templates, Voltage, Droop | | ✔ | | | ✔ | | | | |
| | Jitter Master/Slave Unfiltered | | | ✔ | | | | | | ✔ |
| | Jitter Master/Slave Filtered | | ✔ | ✔ | | | | | | ✔ |
| | Return Loss | ✔ | | | | | | | ✔ | |
| | Common Mode Output Voltage | | | | ✔ | | | | | |
| 100 | Template | | ✔ | | | | | | | |
| | O/p Voltage, Overshoot, Symmetry | | ✔ | | | | | | | |
| | Rise/Fall Time, Rise/Fall Symmetry | | ✔ | | | | | | | |
| | Jitter, Duty Cycle Distortion | | ✔ | | | | | | | |
| | Return Loss | ✔ | | | | | | | ✔ | |
| 10 | MAU Template | | | | | | | ✔ | | |
| | TP_IDL Template | | | | | | ✔ | ✔ | | |
| | Link Pulse Template | | | | | | ✔ | ✔ | | |
| | Jitter | | | | | | ✔ | ✔ | | |
| | Voltage | | | | | | ✔ | | | |
| | Harmonic Content | | | | | | ✔ | | | |
| | Return Loss | ✔ | | | | | | | ✔ | |
| | Common Mode Output Voltage | | | | ✔ | | | | | |

Note 1: RLCF implies Return Loss Calibration Fixture

Note 2: JTC implies Jitter Test Channel

# 3 1000BaseT Compliance Testing

## 3.1 Template, Voltage, and Droop Tests without Disturbing Signal

### 3.1.1 Making Connections

The following connection diagram illustrates the connections required for performing Template, Peak Voltage and Droop tests on your Device Under Test (DUT).

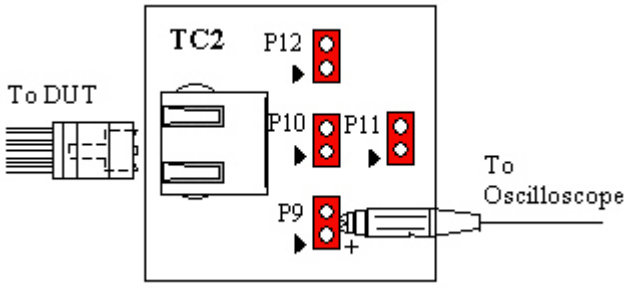



**Figure 1: Connections for 1000BaseT tests without Disturbing Signal**

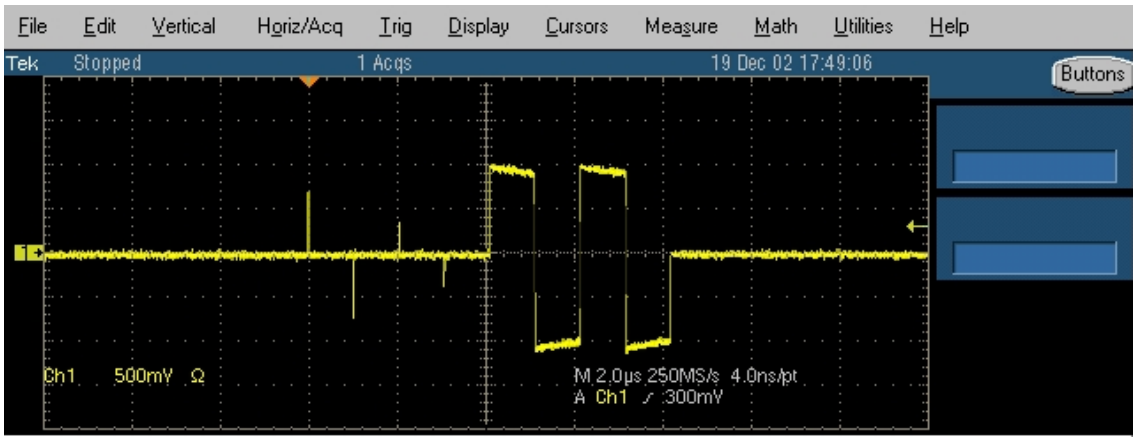
***NOTE.*** *Always align the positive (+) probe-tip of the differential probe with the notch marked on the probing point as shown in the diagram above.*

### 3.1.2 Performing Tests

To perform the tests, follow these steps:

1. Set DUT to generate Test Mode 1 signal.
2. Connect DUT to the Test Fixture as described above.
3. In the TDSET2 software, select 1000-T in the Speed pane.
4. In the Control pane, click on **Reset**.

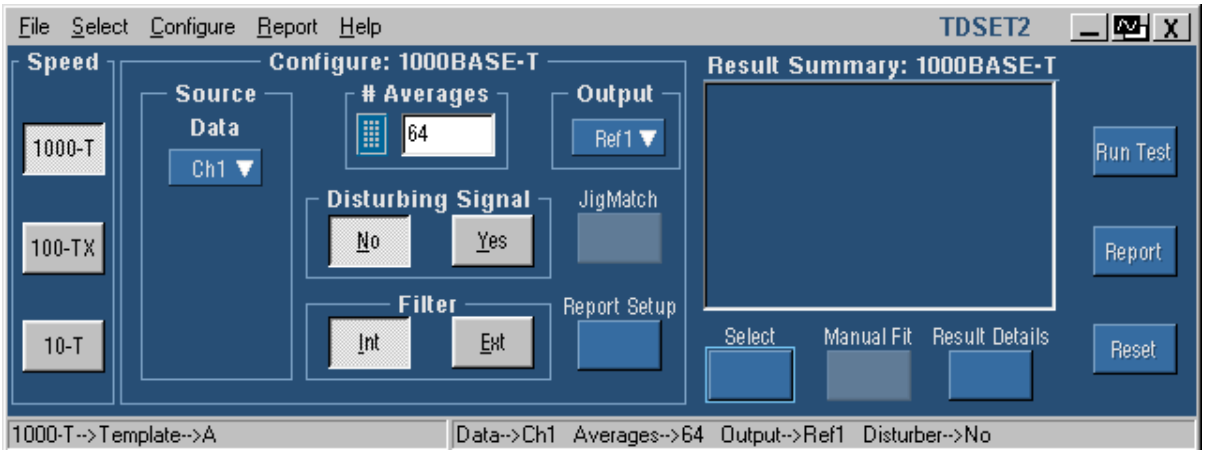
***NOTE****. The first pulse should be going positive. If not, reverse probe connections.*


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Math Utilities Help
Tek Stopped 1 Acqs 19 Dec 02 17:49:06
Buttons
Ch1 500mV Ω
M 2.0µs 250MS/s 4.0ns/pt
A Ch1 ⟋ 300mV

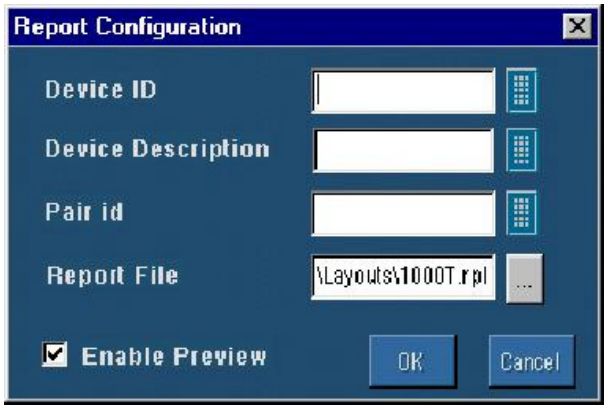
5. In the Template/Volt tab, click **Select All**.

***NOTE**. You can also select one test at a time.*

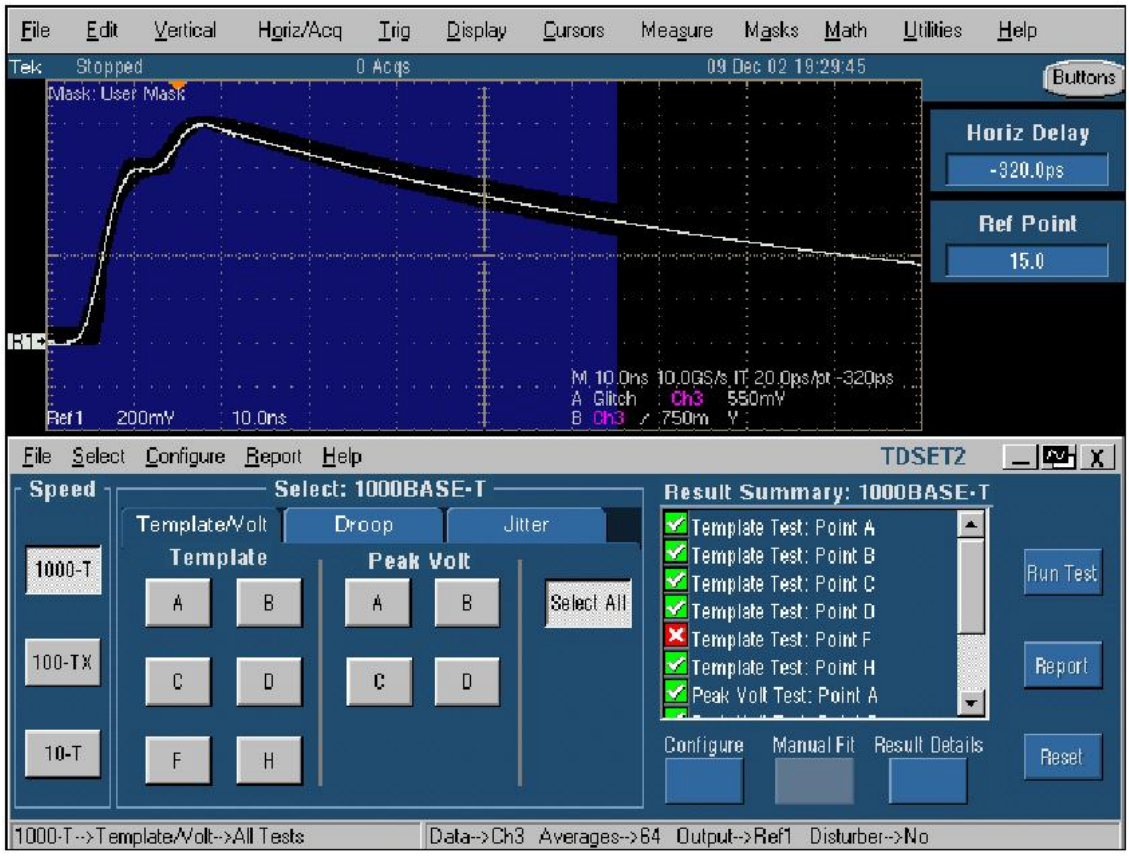
6. Select the **Configure** toggle button in the Control pane to change the configuration settings.
7. To test without disturbing signal, select Disturbing Signal as **No**.




8. Select the data source and set the reference waveform in which the processed waveform will be stored.
9. Select **Report Setup** to configure the report setup to identify and automatically preview the report.




10. Select **Run Test** in the Control pane. The application displays the resulting waveform and the results as pass or fail in the Result Summary pane as shown below.




***NOTE.*** *To manually fit the waveform into the mask, select Manual Fit in the Control pane. You can manually fit only one waveform at a time.*

11. Select **Result Details** in the Control pane for more details.

12. To generate a report automatically, select **Report** in the Control pane.
13. If you want to customize the report format, select **Report > Report Generator**. In the Generate Report tab, select the template and select the **Generate** button to post the test data to the template.
14. For performing Droop tests, click on **Droop** tab and repeat steps 10 through 13.

## 3.2 Template, Voltage, and Droop Tests with Disturbing Signal

### 3.2.1 JigMatch for Accurate Measurements

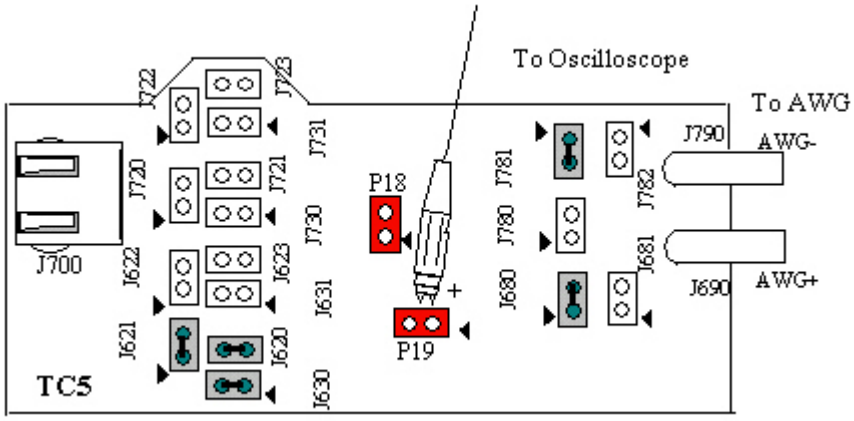
For reliable test results, it is important to remove disturbing signal components accurately. The JigMatch feature ensures that the TDSET2 software compensates for inaccuracies and non-linearities in the Disturbing Signal Generator and the Test Fixture. It is highly recommended that JigMatch is performed every time the Disturber source or the Test Fixture is changed. JigMatch is performed in two steps as described in the following sections.

#### 3.2.1.1 Compensating for Disturbing Signal Generator

**Making Connections**

Set the Disturbing Signal Generator (Disturber) to generate differential 1.4V, 31.25MHz Sine Wave. Connect the outputs of the Disturber to the Test Fixture as shown below.

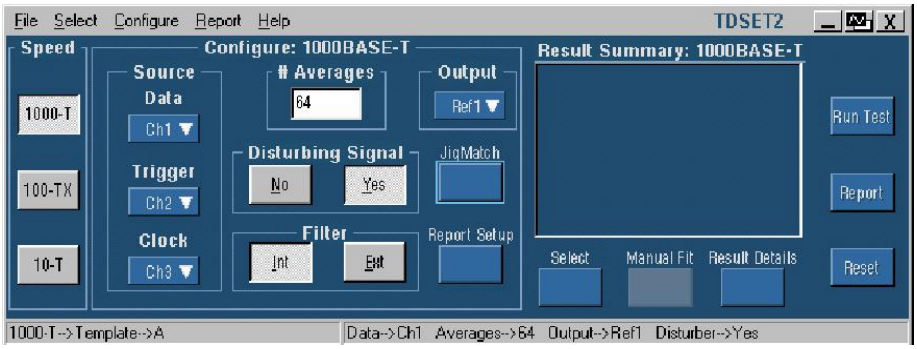
***NOTE.*** *Disconnect the DUT from the Test Fixture if connected.*



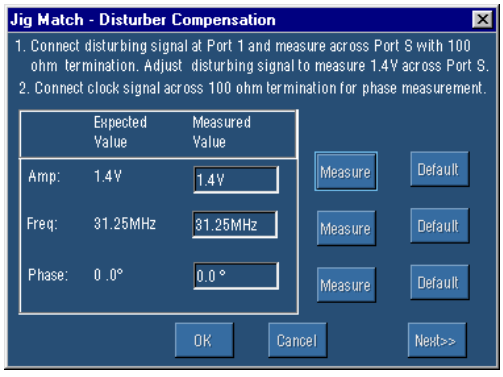

**Performing Disturber Compensation**

1. Select **1000BaseT** in Select pane.

2. Select the **Configure** toggle button in the Control pane to change the configuration settings. Click **Yes** for Disturbing Signal as shown below.




3. Click on **JigMatch**.




4. Click **Measure** buttons to obtain actual ‘Measured’ values.

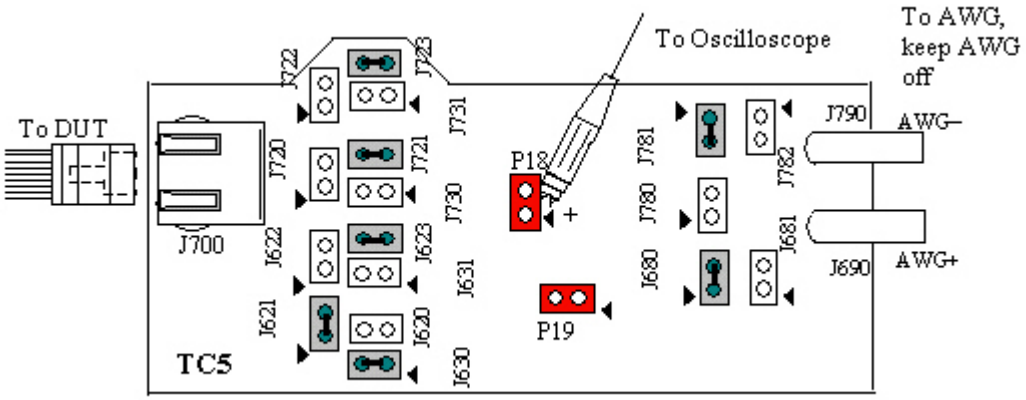
***NOTE**. Ignore Phase measurement if TX_TCLK is not accessible.*

5. Select **OK** to enable the software to compensate for differences.

### 3.2.1.2 Compensating for Test Fixture – DUT Amplitude

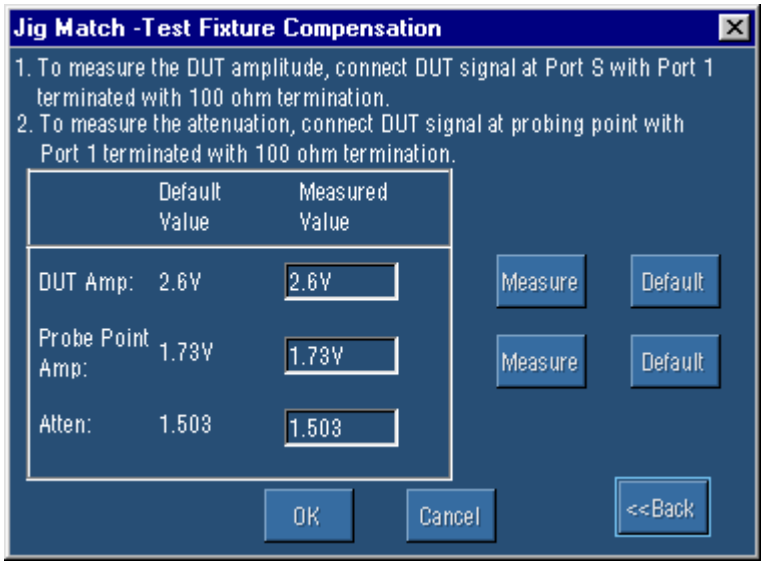
**Making Connections**

1. Set the Device Under Test (DUT) to generate Test Mode 1 signal.
2. Connect the DUT to the Test Fixture using the TF-SIC (short interconnect RJ45 cable) as shown in the picture below.
3. Connect the Disturbing Signal Generator or the Arbitrary Waveform Generator, but switch the outputs OFF.




**Performing Test Fixture Compensation for DUT Amplitude**

1. From the JigMatch screen, select - **Next**.



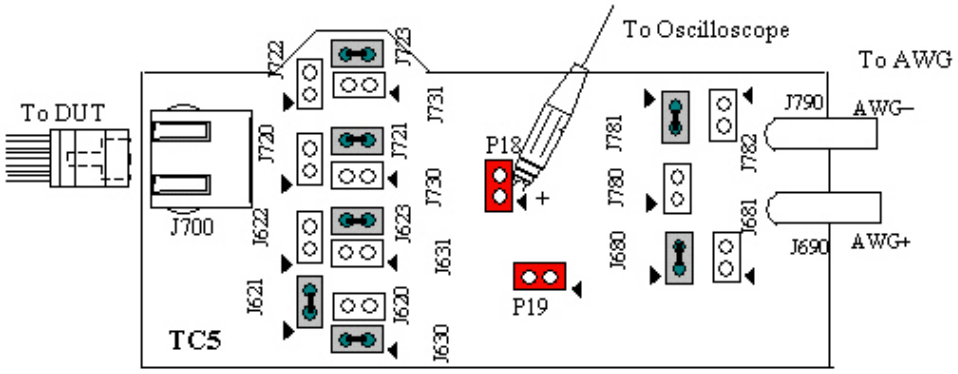

2. Click **Measure** button for Probe Point Amp to obtain actual 'Measured' value.
3. Select **OK** to enable software to compensate for differences.

### 3.2.2 Performing Template Tests

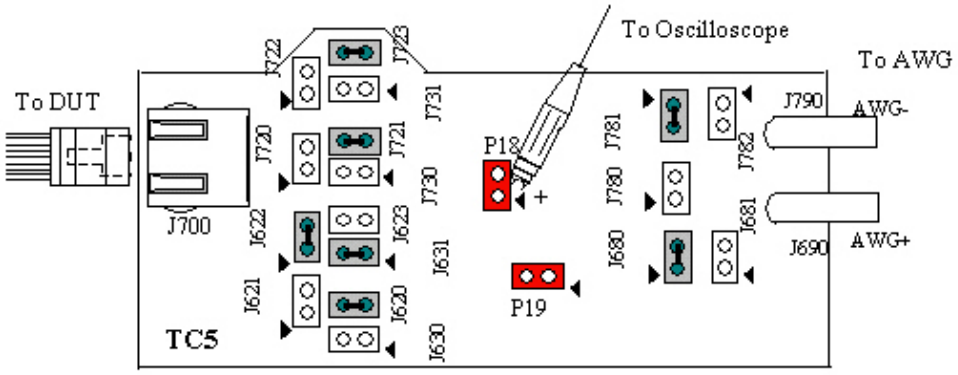
The following sections provide details of connecting and performing template tests with disturbing signal present:

#### 3.2.2.1 Making Connections

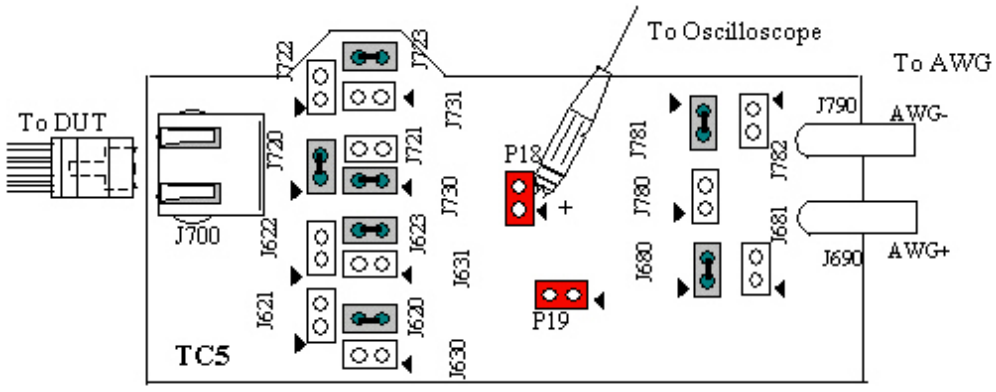
1. For Pair A testing, short J680, J781, J630, J621, J623, J721 and J723. Open the rest. Probe at P18.



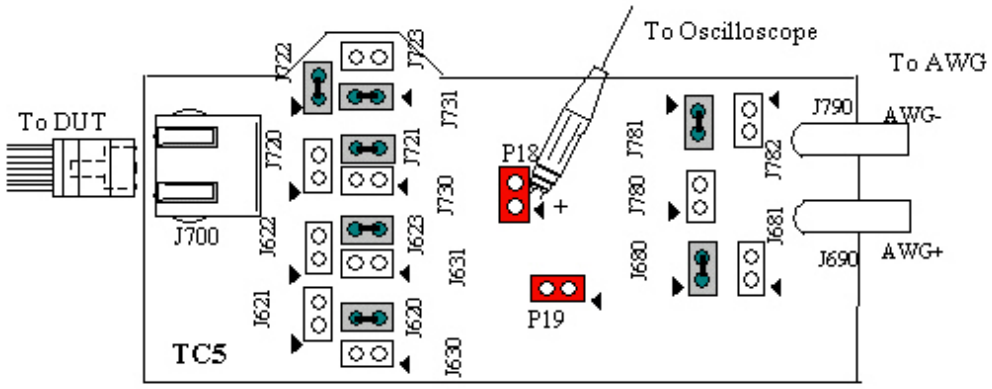

2. For Pair B testing, short J680, J781, J620, J622, J631, J721 and J723. Open the rest. Probe at P18.




3. For Pair C testing, short J680, J781, J620, J623, J720, J730 and J723. Open the rest. Probe at P18.



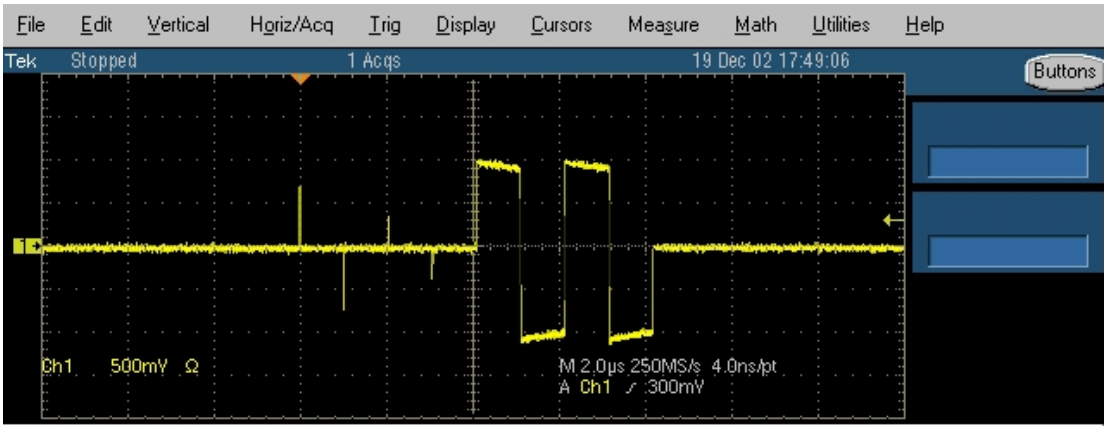
4. For Pair D testing, short J680, J781, J620, J623, J721, J722 and J731. Open the rest. Probe at P18.




### 3.2.2.2 Performing Template Tests

1. Set DUT to generate Test Mode 1 signal.
2. Connect DUT to the Test Fixture as described above.
3. In the TDSET2 software, select 1000-T in the Speed pane.
4. In the Control pane, click on **Reset**.

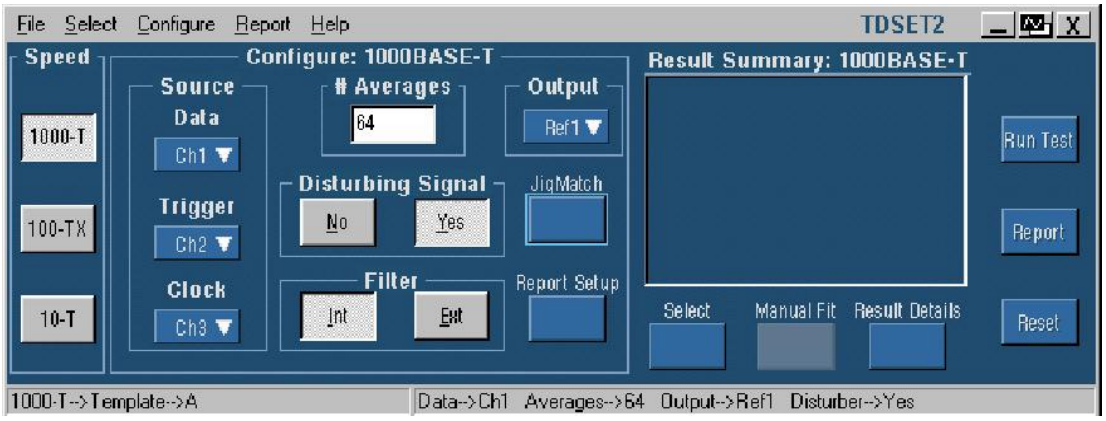
***NOTE**. The first pulse should be going positive. If not, reverse probe connections.*




5. In the Template/Volt tab, click **Select All**.

***NOTE.** You can also select one test at a time.*

6. Select the **Configure** toggle button in the Control pane to change the configuration settings.




7. Select the data source and set the reference waveform in which the processed waveform will be stored.

8. Select **Report Setup** to configure the report setup to identify and automatically preview the report.

9. Select **Run Test** in the Control pane. The application displays the resulting waveform and the results as pass or fail in the Result Summary pane as shown below.

***NOTE.*** *To manually fit the waveform into the mask, select Manual Fit in the Control pane. You can manually fit only one waveform at a time.*

10. Select **Result Details** in the Control pane for more details.

11. To generate a report automatically, select Report in the Control pane.

12. If you want to customize the report format, select Report> Report Generator. In the Generate Report tab, select the template and select the Generate button to post the test data to the template.

13. For performing Droop tests, click on the Droop tab and repeat steps 10 through 13.

## 3.3 Jitter Tests

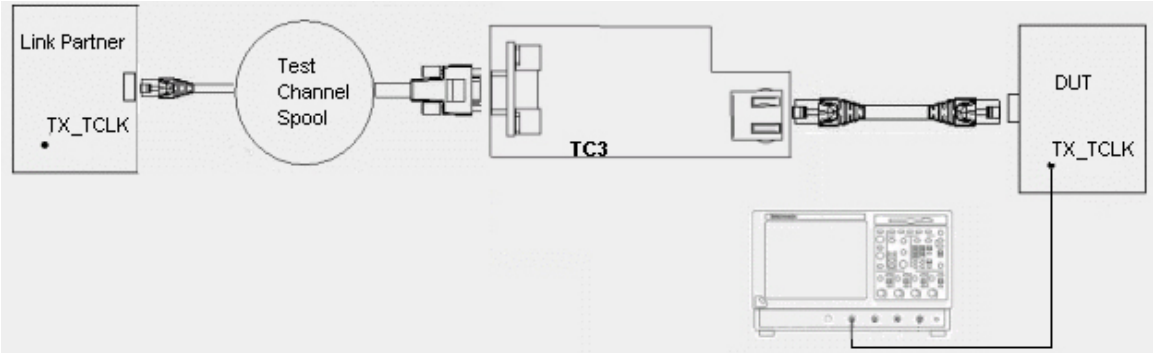
Most of the jitter tests are performed with a Link partner connected. The standard describes a test channel to be used while connecting between the Device Under Test (DUT) and the Link partner. The TF-GBE-JTC Jitter Test Channel is used for connecting between the two ports. Test circuit TC3 provides an adaptor from Sub-D connector on the Test Channel to RJ45 connector for easy connection to a Link partner.

The following sections describe how to perform the jitter tests.

### 3.3.1 Performing Master Unfiltered Jitter Tests

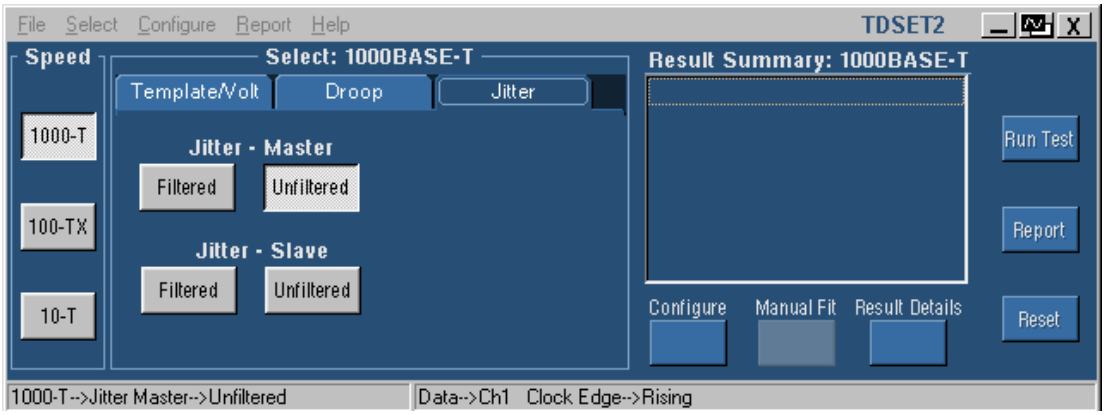
#### 3.3.1.1 Making Connections

1. Set the two devices (DUT and Link Partner) to transmit in Normal Mode.
2. Connect RJ45 connector on the Test Channel (TF-GBE-JTC) to the Device Under Test (DUT).
3. Connect Sub-D connector of the jitter-test-channel to TC3 Sub-D connector.
4. Connect the other end RJ45 connector to the Link Partner using the short interconnect RJ45 cable (TF-GBE-SIC).
5. Connect the probe tip to the Master TX_TCLK on the DUT as shown in picture below.

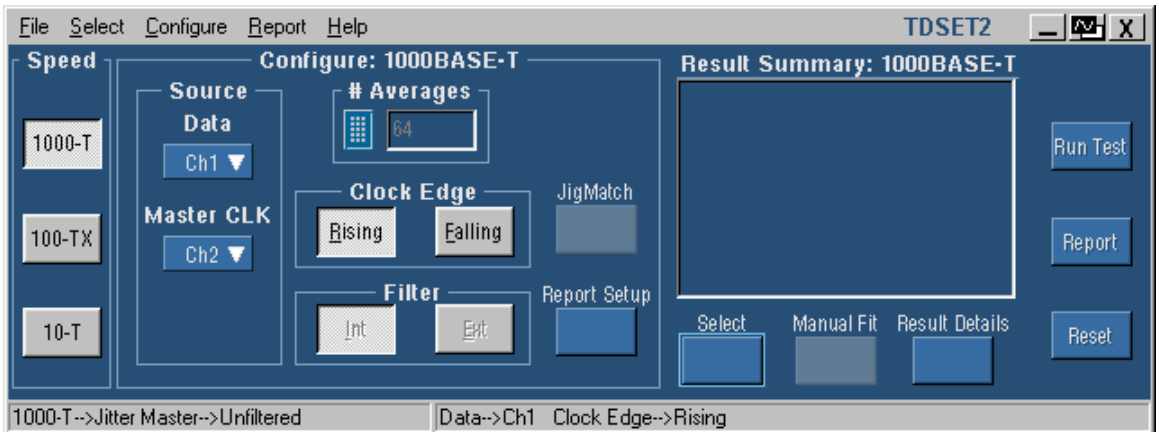



#### 3.3.1.2 Performing Test

1. From the Client pane, select Jitter. Click on **Master Unfiltered** tab.




2. Click the **Configure** button and define the oscilloscope channel to which the Master TX_TLCK is connected.



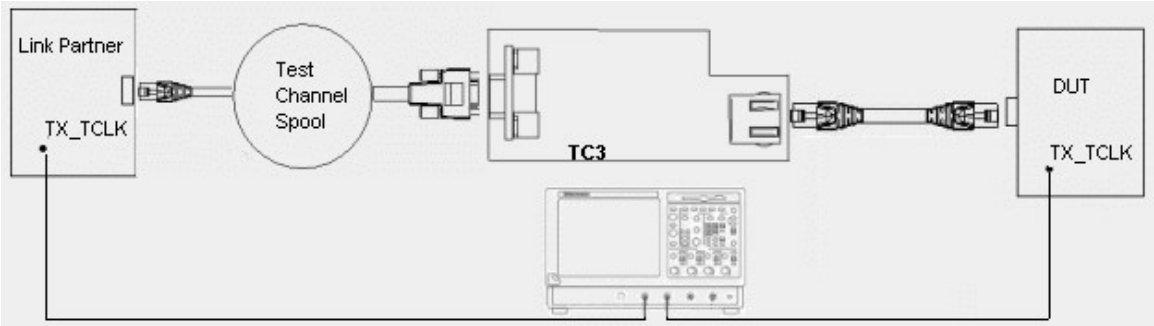

***NOTE.*** *Ignore the Source selection for "Data" as it is not required for this test.*

3. Select **Run Test** in the Control pane. The application displays the resulting waveform and the results as pass or fail in the Result Summary pane as shown below.
4. Select **Result Details** in the Control pane for more details.
5. To generate a report automatically, select **Report** in the Control pane.

### 3.3.2 Performing Slave Unfiltered Jitter Tests

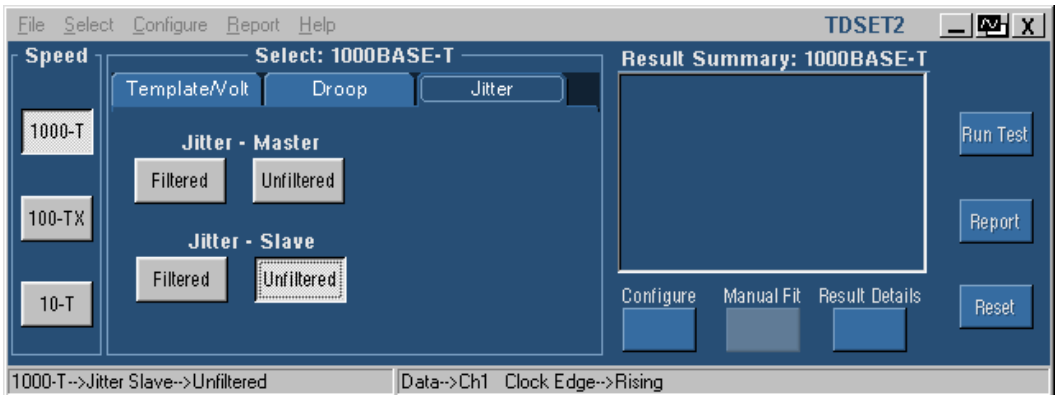
#### 3.3.2.1 Making Connections

1. Set the two devices (DUT and Link Partner) to transmit normally.
2. Connect RJ45 connector on the Test Channel (TF-GBE-JTC) to the Device Under Test (DUT).
3. Connect Sub-D connector of the jitter-test-channel to TC3 Sub-D connector.
4. Connect the other end RJ45 connector to the Link Partner using the short interconnect RJ45 cable (TF-GBE-SIC).
5. Connect the probe tip to the Slave TX_TCLK on the DUT and another probe to the Master TX_TCLK on the Link Partner as shown in picture below.

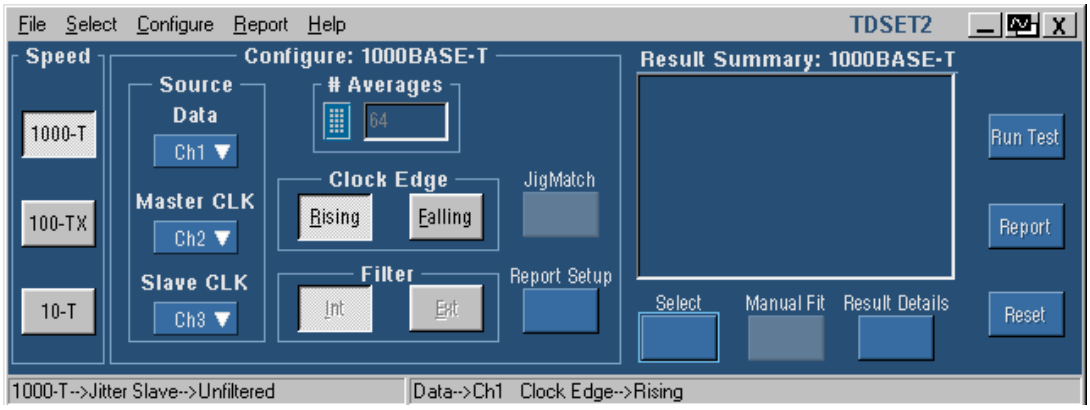



### 3.3.2.2 Performing Test

1. From the Client pane, select Jitter. Click on Slave Unfiltered tab.




2. Click the Configure button and define the oscilloscope channel to which the Slave and Master TX_TLCK are connected.




***NOTE.*** *Ignore the Source selection for "Data" as it is not required for this test.*

3. Select **Run Test** in the Control pane. The application displays the resulting waveform and the results as pass or fail in the Result Summary pane.

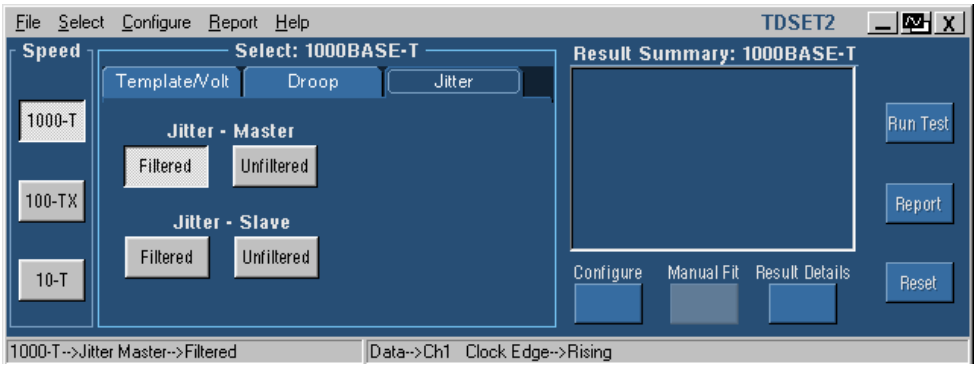
4. Select **Result Details** in the Control pane for more details.

5. To generate a report automatically, select **Report** in the Control pane.

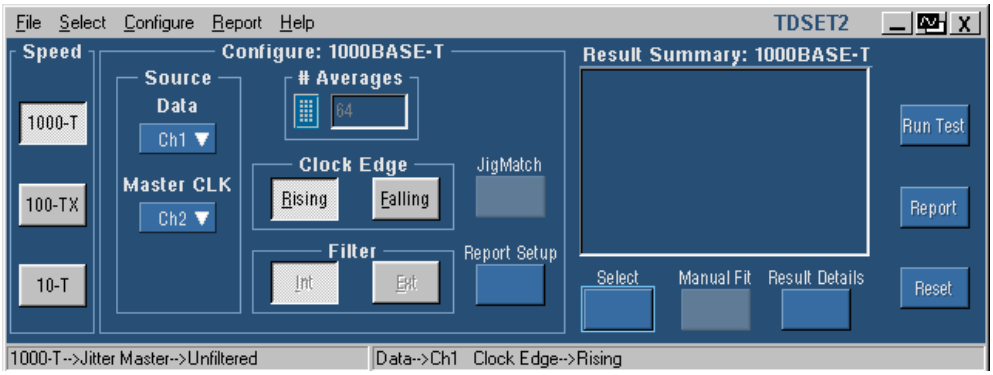
### 3.3.3 Performing Master filtered Jitter Tests

#### 3.3.3.1 Measuring Filtered Jitter on TX_TCLK

1. In the TDSET2, select **Master Filtered Jitter** as shown.

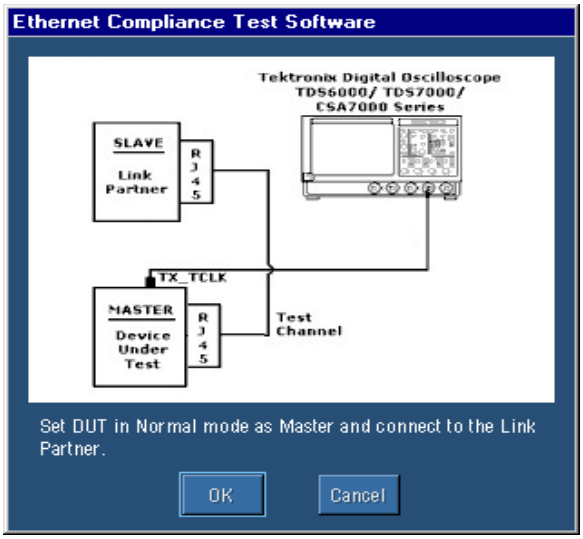



2. Click the **Configure** button and define the oscilloscope channel to which the Master TX_TLCK is connected and the Data channel would be connected.

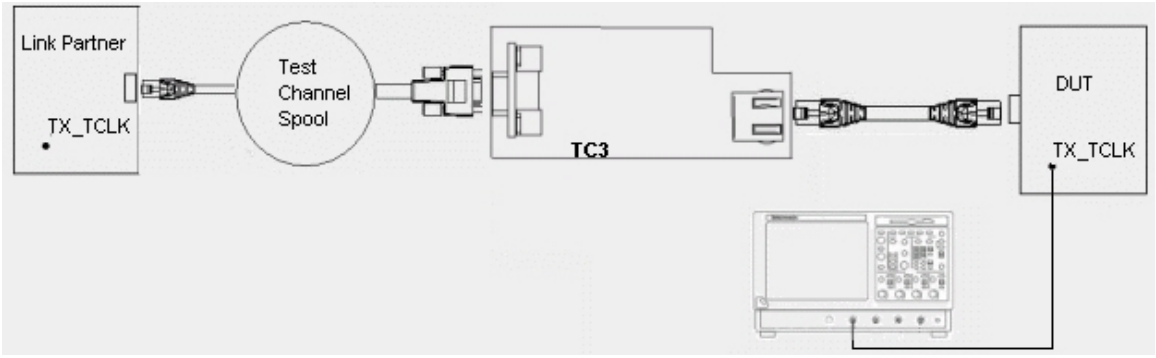



***NOTE.*** *Ignore the Source selection for "Data" as it is not required for this measurement.*

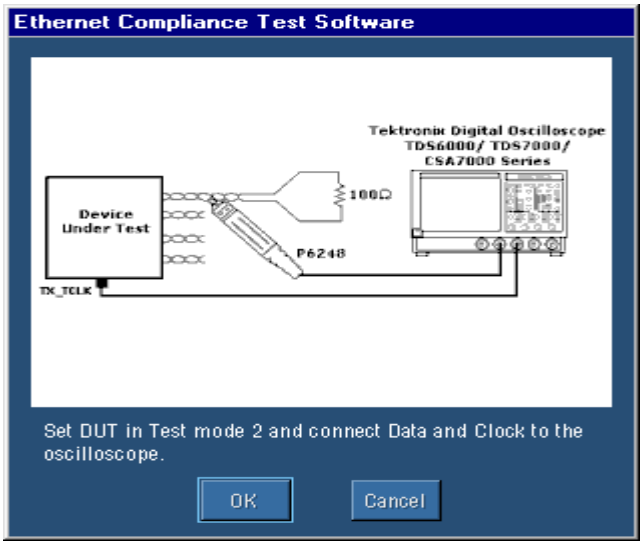
3. Select **Run Test** in the Control pane. A pop-up display that provides connection details would appear.




4. Make connections as described below and later select the **OK** button.



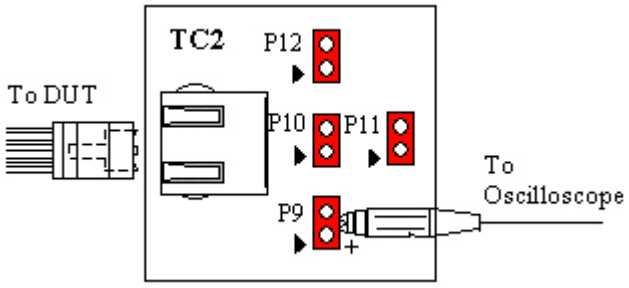

5. Another pop-up dialog giving connection details for Jtxout measurement would appear as depicted below. Refer next section 2.3.3.2 for more details.



#### 3.3.3.2 Measuring Jtxout

1. After completing the steps described in section 2.3.3.1 above, set the DUT to generate Test Mode 2 signal.

2. Connect DUT as shown below:




3. On the oscilloscope screen, select **OK** on the pop-up dialog.

4. The application displays the resulting waveform and the results as pass or fail in the **Result Summary** pane as shown below.

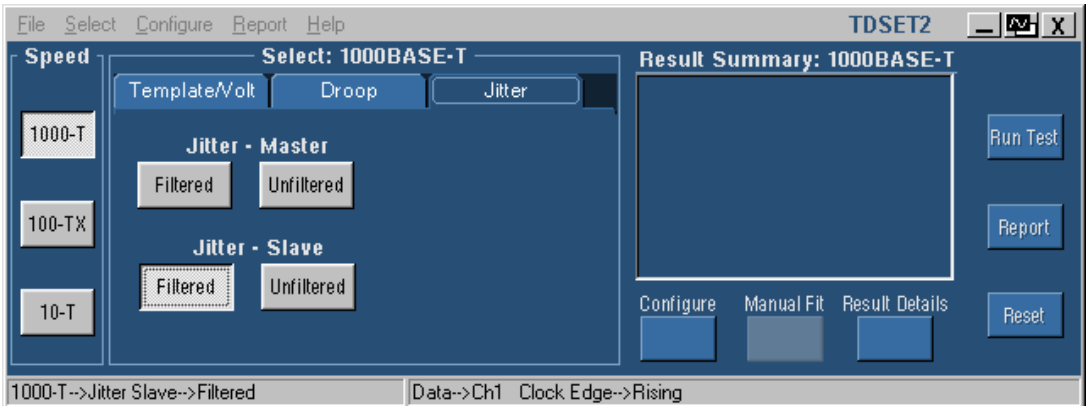
5. Select **Result Details** in the Control pane for more details.

6. To generate a report automatically, select **Report** in the Control pane.

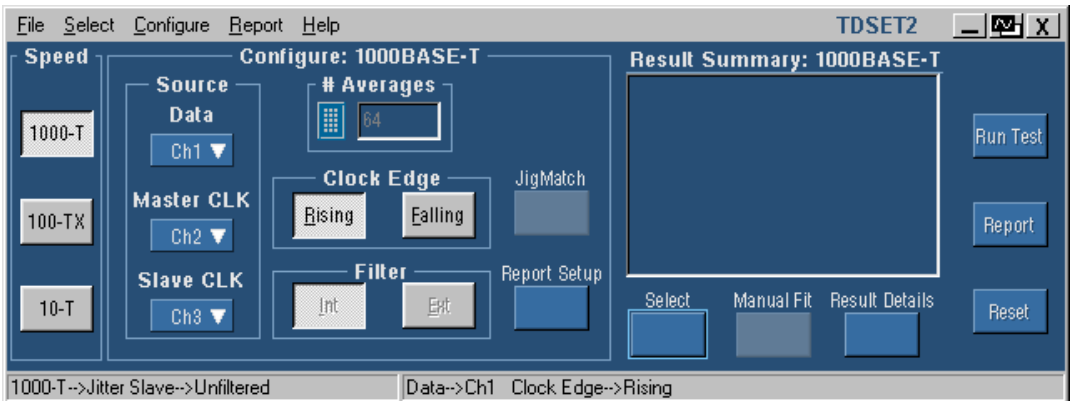
### 3.3.4 Performing Slave filtered Jitter Tests

#### 3.3.4.1 Measuring Filtered Jitter on TX_TCLK

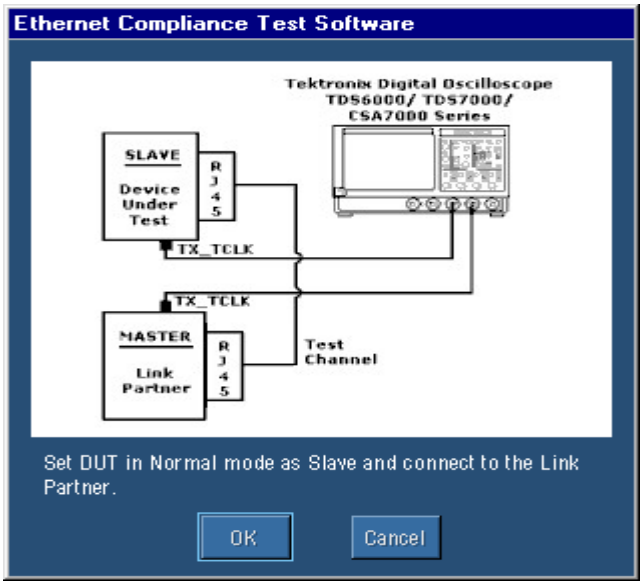
1. In the TDSET2, select **Slave Filtered Jitter** as shown.



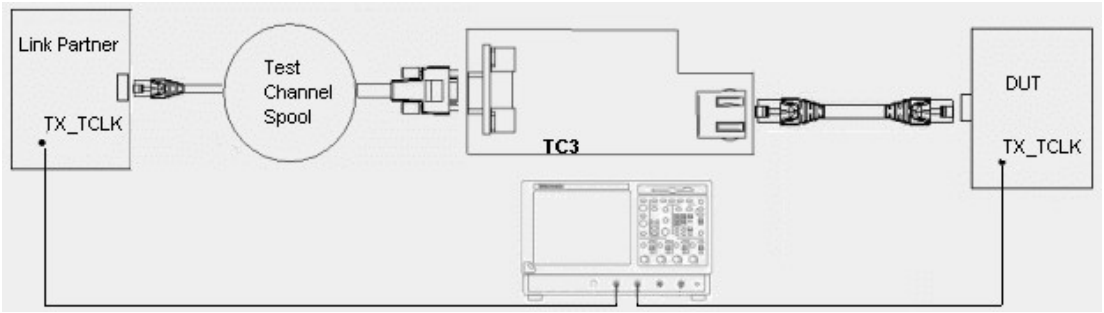

2. Click the **Configure** button and define the oscilloscope channel to which the Slave and Master TX_TLCK are connected and the Data channel would be connected.



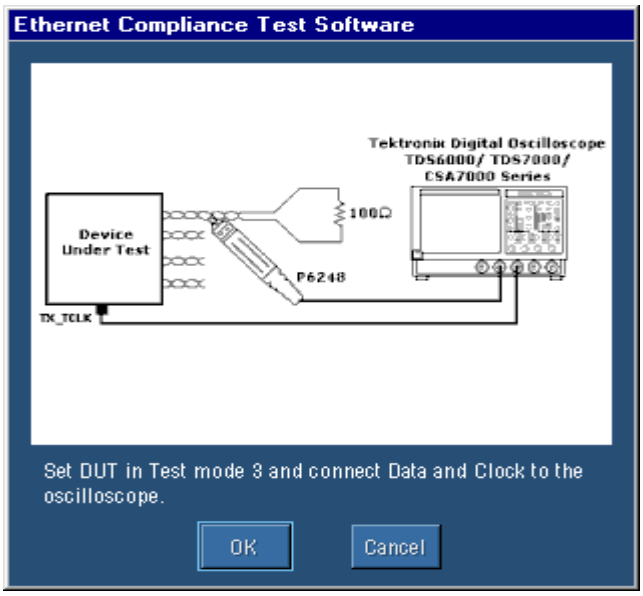

3. Select **Run Test** in the Control pane. A pop-up display that provides connection details would appear.




4. Make connections as described below and later select the **OK** button.

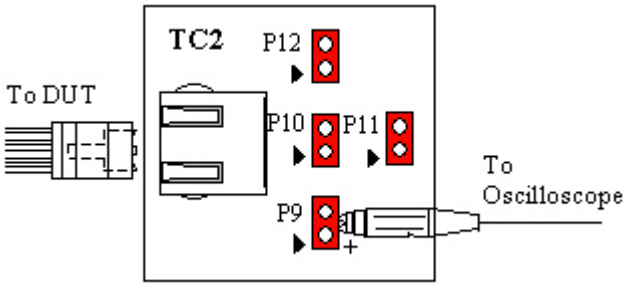



5. Another pop-up dialog giving connection details for Jtxout measurement would appear as depicted below. Refer next section 2.3.4.2 for more details.




### 3.3.4.2 Measuring Jtxout

1. After completing the steps described in section 2.3.4.1 above, set the DUT to generate Test Mode 3 signal.
2. Connect DUT as shown below:




3. On the oscilloscope screen, select **OK** on the pop-up dialog.
4. The application displays the resulting waveform and the results as pass or fail in the **Result Summary** pane as shown below.
5. Select **Result Details** in the Control pane for more details.
6. To generate a report automatically, select **Report** in the Control pane.

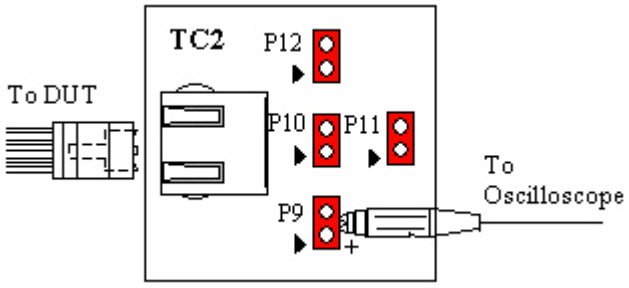
# 4 100BaseTX Compliance Testing

## 4.1 Making Connections

Compliance testing of 100BaseT requires the Device Under Test (DUT) to generate random test packets. This can be accomplished by either using boot software that enables random packet generation or by connecting the DUT to a Link Partner that is generating idle pulses. The following section describes connections for performing tests under each condition.

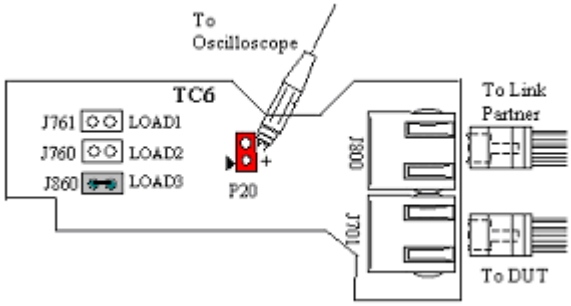
### 4.1.1 Connections with stand-alone port

Connect the DUT as described in the picture below.



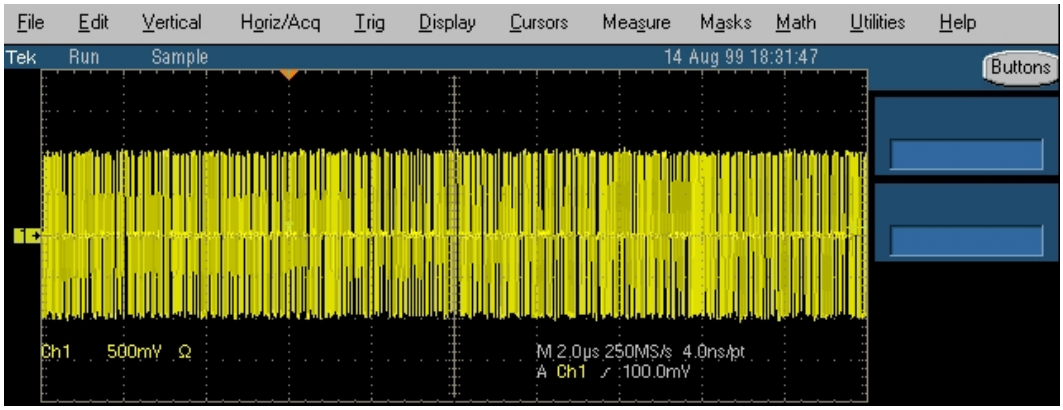

### 4.1.2 Connections when using a link partner

Connect the DUT as described in the picture below.



## 4.2 Performing Tests

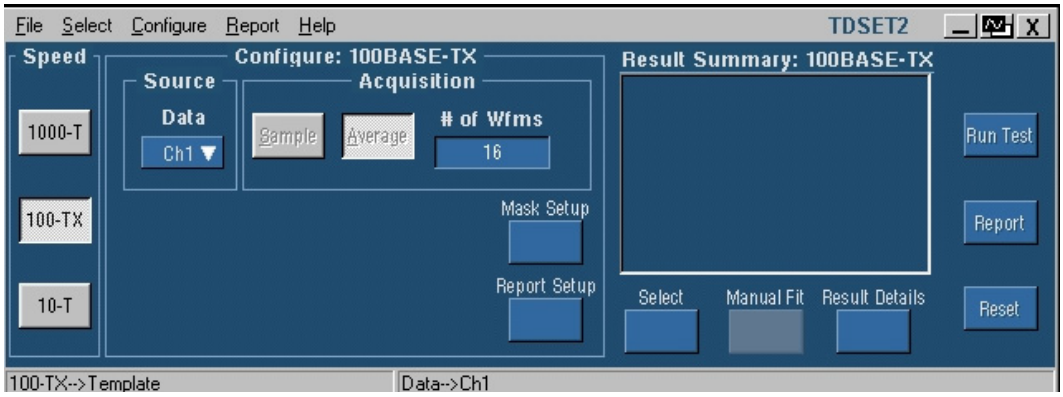
1. Select **100-TX** in the Speed pane. In the Control pane, click on Reset. The random sequence should appear on the screen.


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Masks Math Utilities Help
Tek Run Sample 14 Aug 99 18:31:47
Buttons
Ch1 500mV Ω
M 2.0µs 250MS/s 4.0ns/pt
A Ch1 ⟋ 100.0mV

2. In the Parametric tab, click **Select All**.

***NOTE.*** *You can also select one test at a time.*

3. Select the **Configure** toggle button in the Control pane to change the configuration settings.

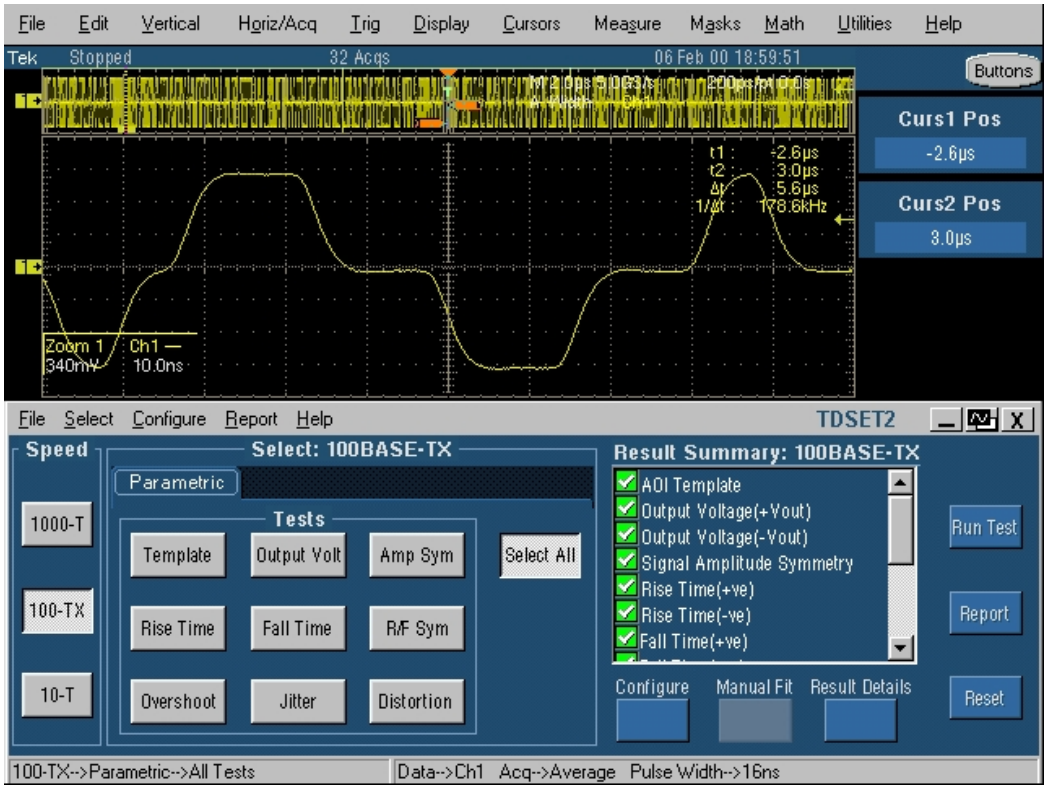



4. Select the data source, number of averages, and mask configuration.

5. Select **Report Setup** to configure the report setup to identify and automatically preview the report.

6. Select **Run Test** in the Control pane.

7. The application displays the resulting waveform and the results as pass or fail in the **Result Summary** pane as shown below.




***NOTE.*** *To manually fit the waveform into the mask, select Template test individually and click Run Test. Select Manual Fit in the Control pane.*

8. Select **Result Details** in the Control pane for more details.

**Result Details: 100BASE-TX**

| Description | Spec Range | Measured Value | Pass/Fail | Remarks |
|---|---|---|---|---|
| AOI Template | Fit the Template | Total Hits = 0 | Pass | |
| Output Voltage(+Vout) | 950mV to 1050mV | 1006.3mV | Pass | - 39.4mV offset con |
| Output Voltage(-Vout) | -950mV to -1050mV | -1020.3mV | Pass | - 39.4mV offset con |
| Signal Amplitude Symmetry | 0.98 to 1.02 | 0.986 | Pass | |
| Rise Time(+ve) | 3.0ns to 5.0ns | 4.17ns | Pass | |
| Rise Time(-ve) | 3.0ns to 5.0ns | 4.14ns | Pass | |
| Fall Time(+ve) | 3.0ns to 5.0ns | 4.14ns | Pass | |
| Fall Time(-ve) | 3.0ns to 5.0ns | 4.24ns | Pass | |
| Rise/Fall Symmetry(+ve) | <500ps | 33.6ps | Pass | |
| Rise/Fall Symmetry(-ve) | <500ps | 114ps | Pass | |
| Overshoot(+ve) | < 5% | 1.60% | Pass | |
| Overshoot(-ve) | < 5% | 0.00% | Pass | |
| Transmit Jitter | < 1.4 ns | 600.0ps | Pass | |
| Distortion(Duty Cycle) | <500ps (+/-250ps) | 200ps | Pass | |

9. To generate a report automatically, select **Report** in the Control pane.

# 5 10BaseT Compliance Testing

10BaseT testing requires special patterns that need to be generated from the DUT port. These tests are carried out using a Twisted Pair Model (also referred to as TPM or cable). The following chart describes the patterns and TPM requirements for various 10BaseT tests:

**Table 5.1: Pattern and TPM requirements for 10BaseT tests**

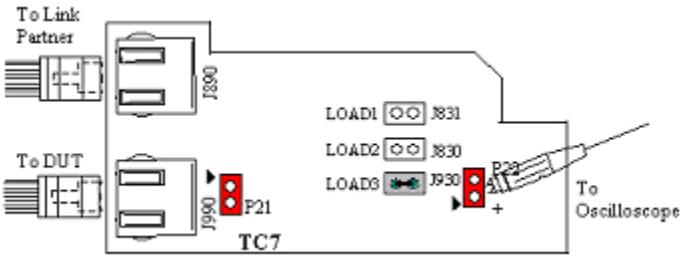
| Test | Pattern required from DUT | With TPM | Without TPM |
|---|---|---|---|
| Link Pulse | Link Pulse | ✔ | ✔ |
| MAU Template | Pseudorandom | ✔ | ✕ |
| TP_IDL | Pseudorandom | ✔ | ✔ |
| Jitter | Pseudorandom | ✔ | ✔ |
| Differential Voltage | Pseudorandom | ✕ | ✔ |
| Harmonic | All 1s or 0s | ✕ | ✔ |

## 5.1 Making Connections

***NOTE1.*** *If the DUT is configured using boot software to generate required test signal, do ignore connection to a Link partner.*

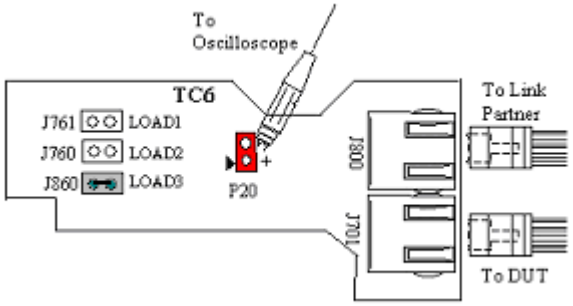
***NOTE2.*** *Load 3 in the TC6 and TC7 circuit is 100 ohm.*

### 5.1.1 With TPM (or cable)




| Test | Load |
|---|---|
| MAU | Load 3 / 100Ω |
| Jitter with cable | Load 3 / / 100Ω |
| Link Pulse | Load 1, 2, 3 |
| TP_IDL | Load 1, 2, 3 |

### 5.1.2 Without TPM (or cable)

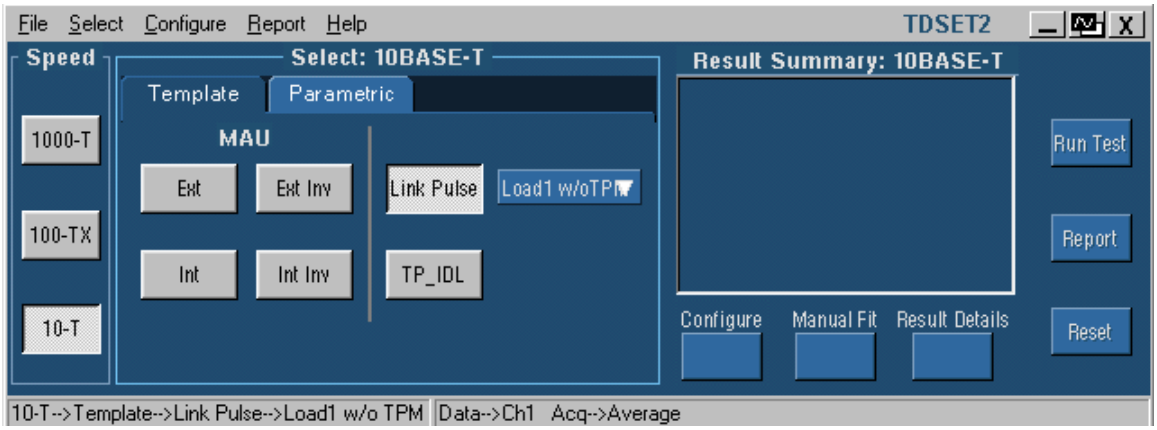



| Test | Load |
|---|---|
| Differential Voltage | Load 3 / 100Ω |
| Jitter without cable | Load 3 / 100Ω |
| Harmonic | Load 3 / 100Ω |
| Link Pulse | Load 1, 2, 3 |
| TP_IDL | Load 1, 2, 3 |

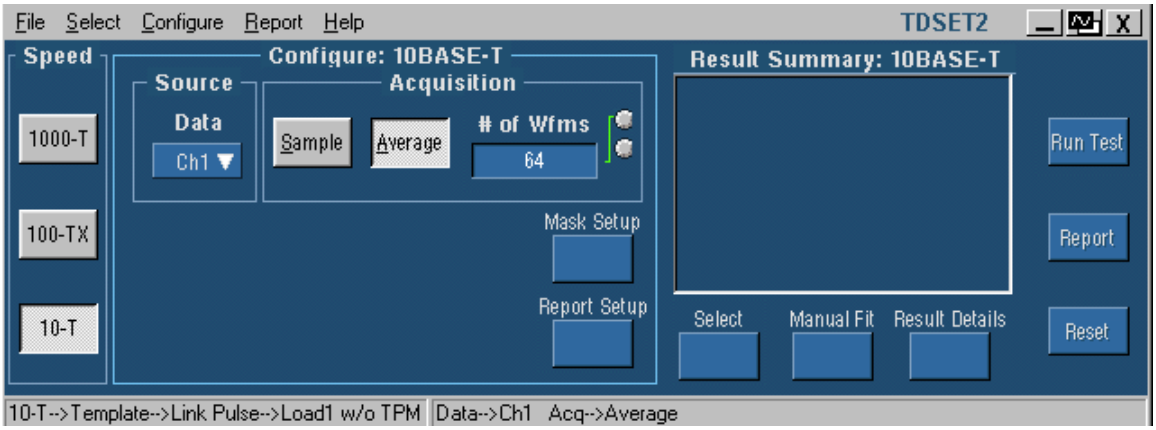
## 5.2 Performing 10BaseT Test

1. Select **10-T** in the Speed pane. Select **Template** in the Client pane. In the Control pane, click on **Reset**.

2. In the Template tab, select desired test. Select **Load w/TPM** in the side pop-up. This example depicts Link Pulse. Other tests can be performed similarly.




3. Select the **Configure** toggle button in the Control pane to confirm or change the configuration settings.

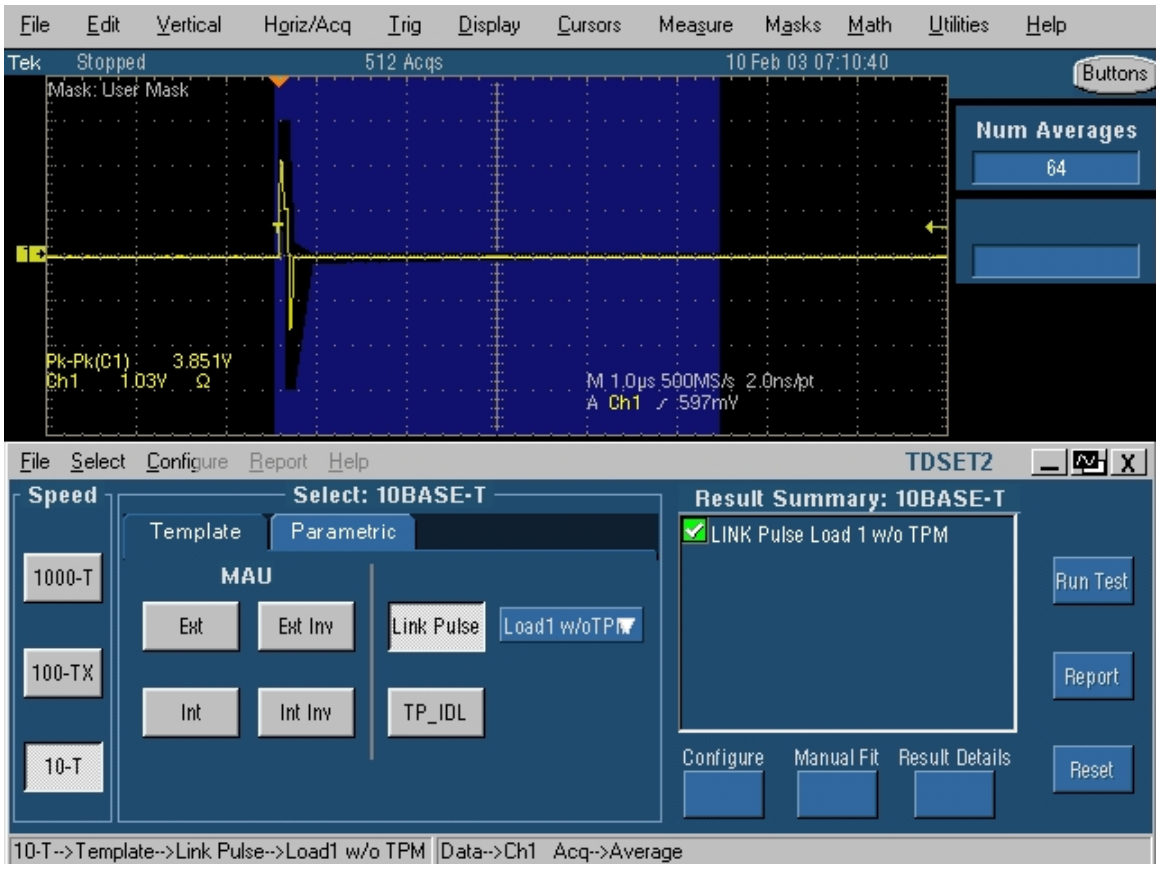



4. Select the data source and number of averages.

5. Select **Report Setup** to configure the report setup to identify and automatically preview the report.

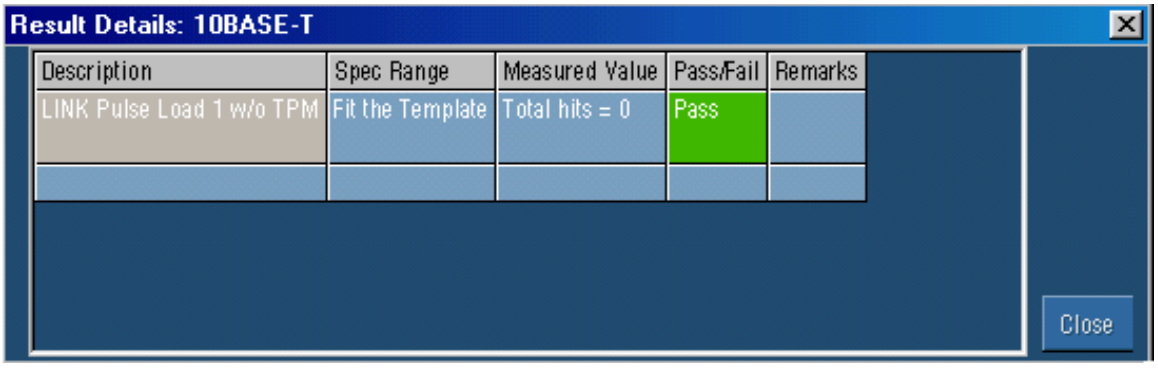
6. Select **Run Test** in the Control pane.

7. The application displays the resulting waveform and the results as pass or fail in the **Result Summary** pane as shown below.




***NOTE.*** *To manually fit the waveform into the mask, select Template test individually and click Run Test. Select Manual Fit in the Control pane.*

8. Select **Result Details** in the Control pane for more details.

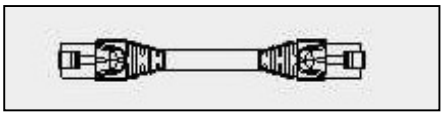



9. To generate a report automatically, select Report in the Control pane.

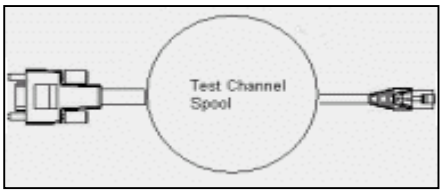
# 6 Accessories and Ordering Information

## 6.1 Test Fixture Accessories

Short Interconnect Cable: TF-GBE-SIC



Jitter Test Channel: TF-GBE-JTC




## 6.2 Test Fixture

Basic Test Package: TF-GBE-BTP

Advanced Test Package: TF-GBE-ATP

## 6.3 Oscilloscope Accessories (contact Tektronix for more details)

Differential Probes: P6247, P6248, P6330, P7330 and P7350

Active Probes: Any Tektronix Active Probe with bandwidth greater than 1GHz.